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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/047,320	03/24/1998	RAYMOND LI	0100.01142	3118

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EXAMINER	
NGUYEN, HAU H	
ART UNIT	PAPER NUMBER
2628	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/047,320	LI, RAYMOND	
	Examiner	Art Unit	
	HAU H. NGUYEN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-24* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/09/2009 has been entered.

Claim Objections

2. Claim 1 is objected to because of the following informalities: Claim 1, line 9, claims the limitation "the *video* graphics processing circuit", which was not introduced before. Appropriate correction is required to avoid lack of antecedent basis.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 6-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. Patent No. 5,774,131) in view of Dutton (U.S. Patent No. 5,802,330).

As per claim 1, as shown in Figs. 2 and 3, Kim teaches *a video graphics and audio processing circuit comprising:*

a graphics processing circuit (151)*;*

an audio processing circuit (156)*;*

a local bus (bus coupled to the control logic 150 from the graphics engine 151 and sound engine 156 inside the coprocessor 15) *operative to receive incoming data from a system bus* (address and data bus coupled to the CPU shown in Fig. 2, the control logic receive data from the system bus via the bus arbitrator and memory controller 14) *and operatively coupled to the graphics processing circuit and the audio processing circuit* (see Fig. 3)*; and*

a bus arbitrator (control logic 150) *operatively coupled to the local bus, the graphics processing circuit, and the audio processing circuit* (Fig. 3)*, wherein the bus arbitrator interprets the incoming data and provides the incoming data to the audio processing circuit or to the video graphics processing circuit* (col. 4, lines 1-20)*, without an intervening bus* (since the claim does not clarify what '*an intervening bus*' is, it can be interpreted as any kind of bus that is not coupled to the local bus).

Kim fails to explicitly teach *the bus arbitrator arbitrates outputting data on the local bus from the graphics processing circuit and the audio processing circuit.* However, this is what Dutton teaches. As shown in Fig. 1, Dutton teaches a computer system, comprising a graphics processor 170, audio processor 172, and a system bus (CPU bus 104), local bus 120, and a bus arbiter 180 to arbitrate the ownership of different devices including the graphics processor and the audio processor on the local bus 120 (col. 4, lines 18-36).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Dutton in combination with the method as taught by Kim in order to allow real time devices to obtain adequate access to the system busses and the bus arbitration is dynamically varied to account for varying requirements of the system (col. 2, lines 14-17).

As per claim 2, Kim teaches *the bus arbitrator comprises an address decoder operatively coupled to receive an address via the local bus, to route received data to the audio processing circuit when the address identifies the audio processing circuit and to route received data to the graphics processing circuit when the address identifies the graphics processing circuit* (see col. 4, lines 40-55).

As per claim 3, as cited above, Kim does teach the address decoder comprises control circuitry that generates an output data control signal based on the address and a data command signal (col. 4, lines 35-55).

As per claim 4, Kim further teach the bus arbitrator further comprises an output data switch operatively coupled to output data to the bus from the audio processing circuit or the graphics processing circuit based on the output data control signal (i.e. the output of the sound engine and the graphics engine to the address FIFO 154 and the data FIFO 155 is based on the control of the control logic 150, as cited above with reference to Fig. 3).

As per claim 6, as cited above, Kim teaches *a method for bus arbitration between an audio processing circuit and a graphics processing circuit* (Fig. 3)*, the method comprises*

a) receiving at least one address (receiving address from the CPU, col. 4, lines 35-55)*;*

b) determining whether the at least one address identifies at least one of: the audio processing circuit and the graphics processing circuit (this is done by the control logic 150 as cited above) *; and*

c) when the at least one address identifies both the audio processing circuit and the graphics processing circuit (since Kim teaches the sound and graphics data is stored in the same system memory (Fig. 2), and further teaches the timing of audio data and graphics data

transferred into and out of the system memory is display timing signal, it is implied that there's a chance an address in the system memory identifies both sound engine and graphics engine).

Kim fails to teach *arbitrating access to a local bus coupled to the audio processing circuit and the graphics processing circuit without an intervening bus*. However, as cited above referring to claim 1, Dutton teaches this feature.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Dutton in combination with the method as taught by Kim in order to allow real time devices to obtain adequate access to the system busses and the bus arbitration is dynamically varied to account for varying requirements of the system (col. 2, lines 14-17).

As per claim 7, as shown in Fig. 2, since the data provided from the CPU includes data, address and controls, it is implied that Kim teaches (a) further comprises receiving an associated command for each of the at least one address. Dutton also teaches this feature (see col. 5, lines 15-25, and col. 6, lines 50-67). Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Dutton in combination with the method as taught by Kim in order to set the priority of the devices (audio or graphics processing devices) in association with an assigned address.

As per claims 8 and 10, as cited above and shown in Figs. 2-3, Kim teaches enabling the audio processing circuit to receive incoming data via the local bus when at least one address identifies the audio processing circuit (as cited above) and when the associated command is for inputting/outputting data.

As per claims 9 and 11, as cited above, Kim teaches enabling the graphics processing circuit to receive incoming data via the local bus when at least one address identifies the graphics processing circuit and when the associated command is for inputting/outputting data (i.e. write/read data).

As per claim 12, it is inherent that the at least one address comprises a plurality of addresses.

As per claim 13, although not taught by Kim, Dutton teaches intermixing the audio processing circuit's access to the local bus with the graphics processing circuit's access to the local bus based on the plurality of addresses and the associated command (depending on the priority level of the request device).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Dutton in combination with the method as taught by Kim in order to allow real time devices to obtain adequate access to the system busses and the bus arbitration is dynamically varied to account for varying requirements of the system (col. 2, lines 14-17).

As per claim 14, as addressed in claims 6 and 7, Kim in combination with Dutton, teaches a video graphics and audio processing circuit comprising:
a processing unit (15, Fig. 2); and
memory (12) operatively coupled to the processing unit, wherein the memory stores programming instructions that, when read by the processing unit, cause the processing unit to receive at least one address and an associated data command for each of the at least one address; audio process the associated data command when the at least one address identifies audio

processing, and graphics process the associated data command when the at least one address identifies graphics processing.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Dutton in combination with the method as taught by Kim in order to set the priority of the devices (audio or graphics processing devices) in association with an assigned address.

As per claim 15, as cited above, Kim-Dutton in combination teaches the memory further comprises programming instructions that cause the processing unit to determine whether the associated data command is for inputting data or outputting data (i.e. command to write or read data).

Claim 16, which is similar in scope to claim 13, is thus rejected under the same rationale.

Claim 17, which is similar in scope to claims 6 and 14, is thus rejected under the same rationale.

Claims 18-23, which are similar in scope to claims 7-11, and 13, are thus rejected under the same rationale.

As per claim 24, although the combined Kim-Dutton does not explicitly teach the graphics processing unit, the audio processing unit, and the bus arbitrator are configured on a single chip, it would have been obvious to one skilled in the art to integrate all these components into a single chip since by doing so, the circuit can be more compact, and less bus wiring.

Allowable Subject Matter

5. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art taken singly or in combination does not teach or suggest, a video graphics and audio processing circuit, among other things, comprising a multiplexor operatively coupled to the audio buffer and the graphics buffer, wherein the multiplexor outputs the audio output data or the graphics output data based in the output data control signal.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information

about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Hau H Nguyen/

Primary Examiner, Art Unit 2628